

(19)



JAPANESE PATENT OFFICE

PATENT ABSTRACTS OF JAPAN

(11) Publication number: **62142341 A**

(43) Date of publication of application: 25.06.87

(51) Int. Cl.

**H01L 25/04**

(21) Application number: **60283618**

(22) Date of filing: 17.12.85

(71) Applicant: **MATSUSHITA ELECTRONICS  
CORP**

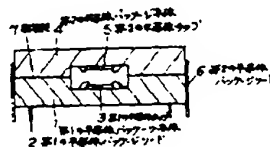
(72) Inventor: **NAKAGAWA SHOICHI**

**(54) SEMICONDUCTOR DEVICE AND  
MANUFACTURE THEREOF**

**(57) Abstract:**

**PURPOSE.** To improve packaging density of a substrate, by a two-stage structure even for a package having a normal size.

**CONSTITUTION:** In a recess part in the surface of a main body of a first semiconductor package 1, die mounting and wiring are performed for a first semiconductor chip 3 by a normal method. A first semiconductor package lead 2 is protruded downward vertically from the surface of the main body of the first semiconductor package. In the recess in the surface of a main body of a second semiconductor package 4, die mounting and wiring are conducted for a second semiconductor chip 5 by a normal method. A second semiconductor package lead 6 is provided on the side surface of the main body of the second semiconductor package 4 on the side of the recess part. Then the surface of the main body of the first semiconductor package 1 other than the recess part on the side of the recess part is bonded to the surface of the main body of the second semiconductor package 4 with a soldering material or a bonding agent 7 in an airtight manner. Thus, the semiconductor device for high packaging density in two-stage structure is completed.



COPYRIGHT: (C)1987,JPO&Japio